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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

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|---|-------------|---|----------|----------------------------------|------------|
| APPL NUM | FILING DATE | CLASS | SUBCLASS | GAU | EXAMINER |
| 10007300 | 11/08/2001 | 257 | 5 | 2811 | THIEN TRAN |
| **APPLICANTS: Jono Keiji; Ueda Hirokazu; Watanabe Hiroyuki; | | | | | |
| **CONTINUING DATA VERIFIED: THIS APPLICATION IS A DIV OF 09/652,550 08/31/2000 YES TT | | | | | |
| ** FOREIGN APPLICATIONS VERIFIED: NONE TT | | | | | |
| PG-PUB <input type="checkbox"/> | | DO NOT PUBLISH <input type="checkbox"/> | | RESCIND <input type="checkbox"/> | |
| Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no | | 35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no | | ATTORNEY DOCKET NO | |
| Verified and Acknowledged Examiners's initials TT | | KM1-003 | | | |
| TITLE : Methods of forming an isolation trench in a semiconductor, methods of forming an isolation trench in a surface of a silicon wafer, methods of forming an isolation trench-isolated transistor | | | | | |
| U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94) | | | | | |

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|--|-----------|-----------------------|----------------------|
| NOTICE OF ALLOWANCE MAILED | | CLAIMS ALLOWED | |
| | | Total Claims | Print Claim for O.G. |
| ISSUE FEE | | DRAWING | |
| Amount Due | Date Paid | Sheets Drwg. | Figs. Drwg. |
| | | Print Fig. | |
| <input type="checkbox"/> TERMINAL DISCLAIMER | | Primary Examiner | |
| | | PREPARED FOR ISSUE | |
| | | Application Examiner | |
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